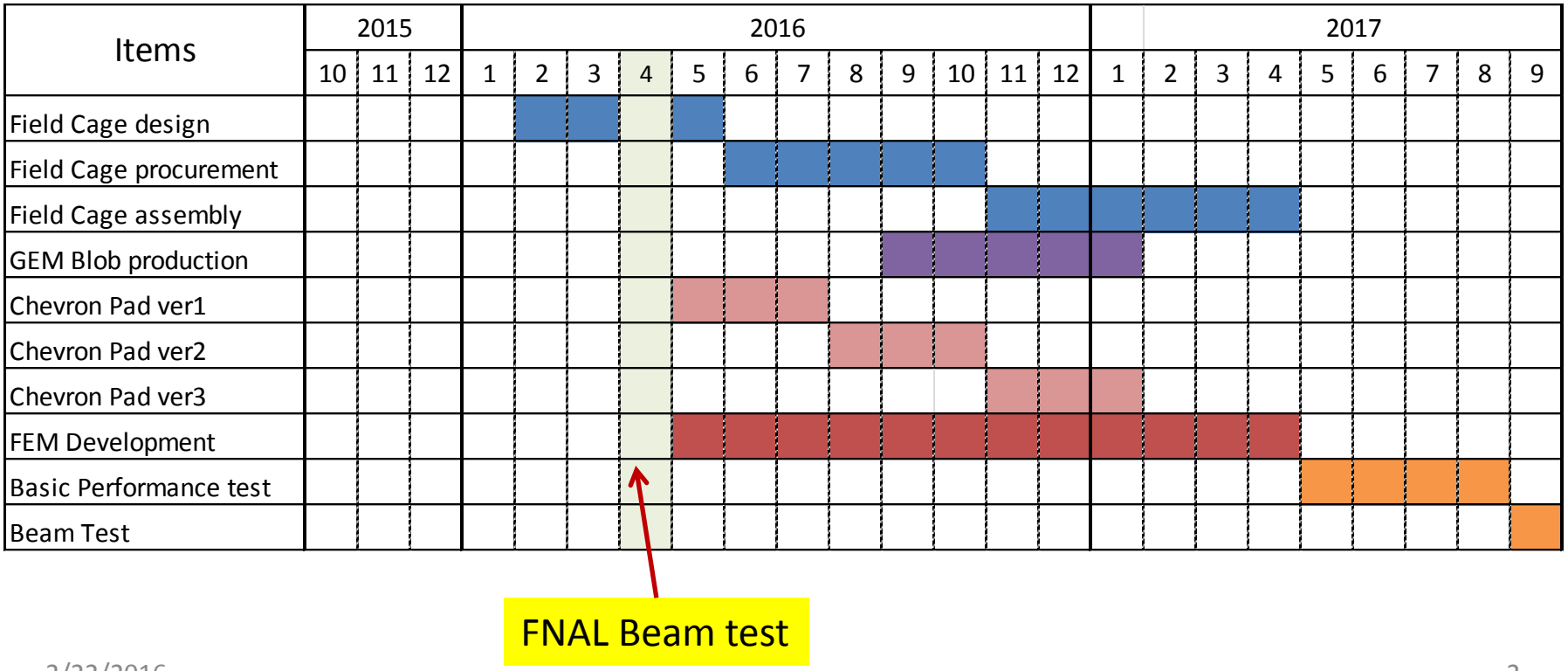
TPC readout electronics discussion (cont'd)

Takao Sakaguchi

Readout situation

- We need electronics to readout. Based on the schedule outlined below, the electronics should be ready by the end of April next year
  - Roughly, one year from now

- We may want to establish a readout scheme that is also good for the final version if possible

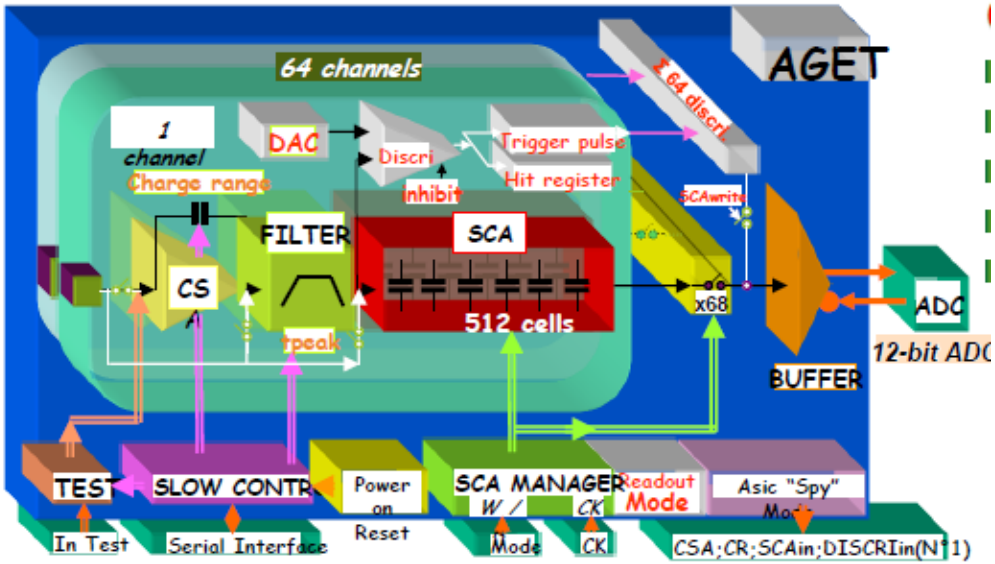


Possible options

- ALICE TPC – uses SAMPA chips
  - We will hear from Ken more detail on the progress today
- STAR iTPC – also uses SAMPA chips
  - They are expecting to receive proto-type of SAMPA chips this April.
  - If they figured out that they can't receive in time, they will reuse current TPC electronics (PASA+ALTRO). We need polarity-change amp. in addition.
  - They will decide in April which way to go.
- DREAM option
  - For test experiments, we can use a board that can handle 512 channels (they are willing to lend us). TS will visit Sacley and learn how to use it.
  - For mass production, we have to discuss with Sacley people about the cost
- ATLAS VMM option (John pointed it to me)
  - An ASIC called VMM is developed here in BNL, and intended to be used both for negative (e.g. Micromegas) and positive signals
  - Haven't contacted to the people involved.
  - Can be operated in continuous mode at 1MHz/channel, 10bit ADC.
  - Needs engineering for peripheral circuit and board design

DREAM – successor of AGET

- Accept bipolar signal. One chip handles 64 channels
  - Four dynamic ranges: 50, 100, 200 and 600 fC (SAMPA: 100 fC)
  - 16 shaping time selection in 50 to 900nsec (SAMPA: 80 or 160nsec peaking)
  - Can handle detector capacitor up to 100pF
- 50MHz sampling with switched capacitor array (SCA, similar to AMU)
  - 512 samples can be stored
  - SCA values can be readout at 20MHz (SAMPA: 20MHz sample rate, no buffer)
  - External trigger and self-trigger can be chosen.
- It can be operated at 1T magnetic field, but not rad-hard



- Based on T2K TPC experience (125K channel), each channel would cost 3-4 euro excluding engineering costs, R&D and manpower → $1M for 200K
- They can provide us either prototype electronics system or some left-over from the CLAS12 production

ATLAS VMM

- Can be operated at 1MHz/channel.
- Continuous mode or (self-)trigger mode can be selected
- Need big engineering, I suppose. We need to talk to ATLAS people

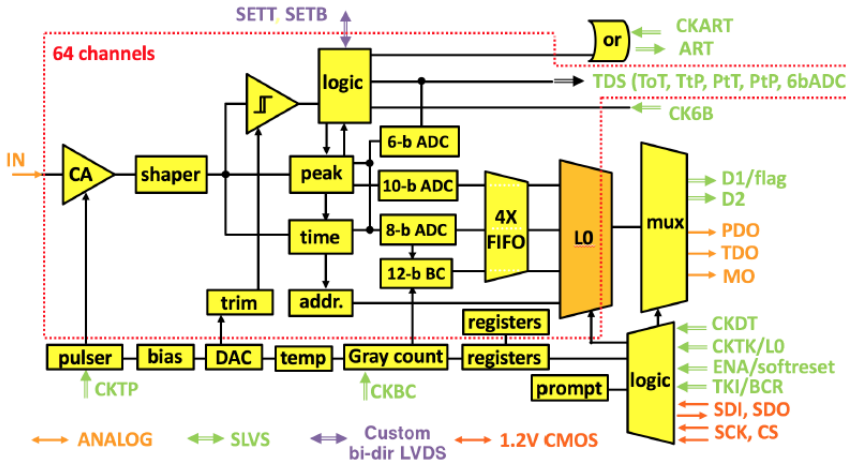


Figure 1: Architecture of VMM3.

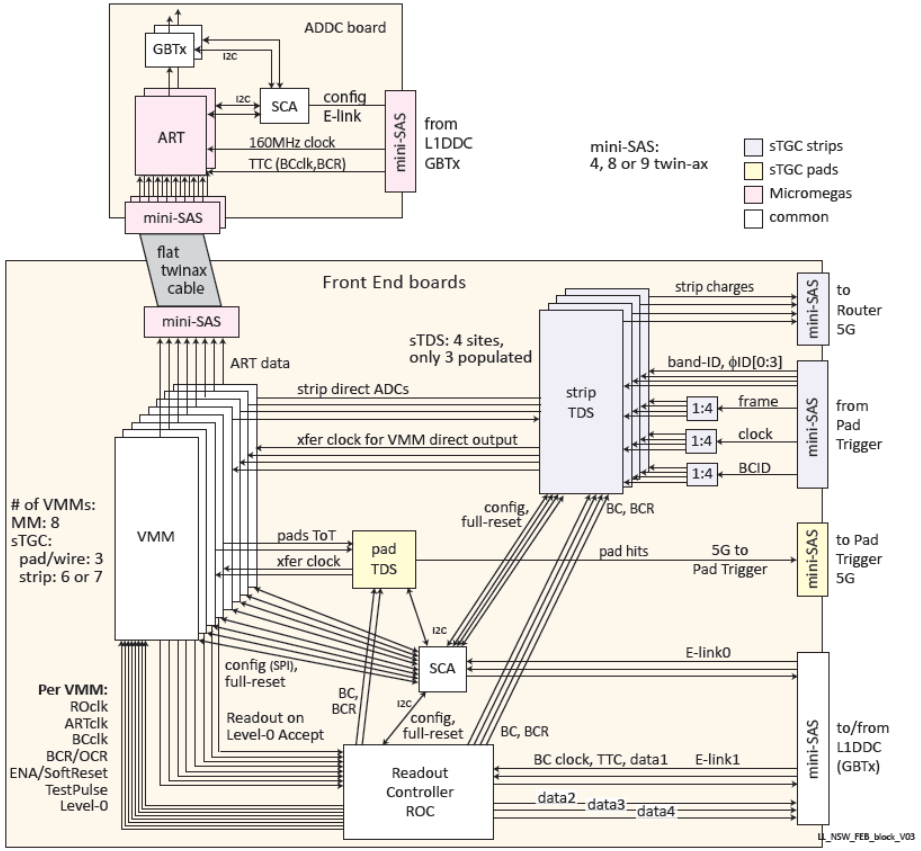
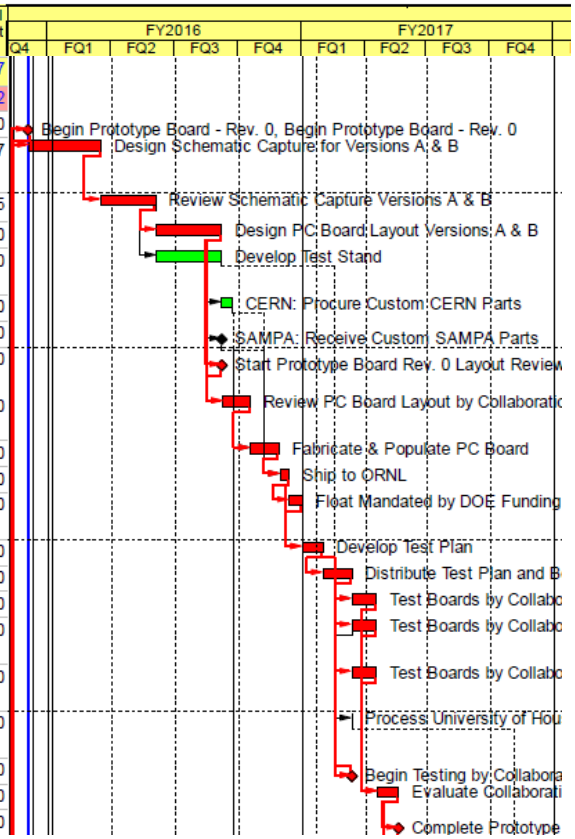


Figure 2: Overall connection diagram of the VMM.

ALICE schedule from WBS last year

- The very first version of proto-type will be produced by the end of FY16
  - I thought they will produce ~10% of total. I should check
- One option is to join the test board effort?

Activity ID	Activity Name	Rem Dur	Start	Finish	Total Float	Budgeted Total Cost
ALICE 1.1.2	Electronics	742d	01-Oct-2015	28-Sep-2018	0d	$3,158,369.87
ALICE 1.1.2.1	Prototype Board - Rev. 0	360d	01-Oct-2015	20-Mar-2017	0d	$480,100.52
TPC-E-Mi10	Begin Prototype Board - Rev. 0	0d	01-Oct-2015		0d	$0.00
TPC-E-1110	Design Schematic Capture for Versions A & B	66d	02-Oct-2015	13-Jan-2016	0d	$121,153.47
TPC-E-1120	Review Schematic Capture Versions A	55d	14-Jan-2016	01-Apr-2016	0d	$100,718.45
TPC-E-1130	Design PC Board Layout Versions A & B	66d	04-Apr-2016	06-Jul-2016	0d	$56,743.00
TPC-E-1140	Develop Test Stand	66d	04-Apr-2016	06-Jul-2016	124d	$122,203.60
TPC-E-1160	CERN: Procure Custom CERN Parts	12d	07-Jul-2016	22-Jul-2016	17d	$6,180.00
TPC-E-Mi12	SAMPA: Receive Custom SAMPA Parts	0d	07-Jul-2016		29d	$0.00
TPC-E-Mi15	Start Prototype Board Rev. 0 Layout Review by Collaboration	0d	07-Jul-2016		0d	$0.00
TPC-E-1150	Review PC Board Layout by Collaboration	28d	08-Jul-2016	16-Aug-2016	0d	$0.00
TPC-E-1180	Fabricate & Populate PC Board	30d	17-Aug-2016	28-Sep-2016	0d	$20,660.00
TPC-E-1190	Ship to ORNL	10d	29-Sep-2016	12-Oct-2016	0d	$530.00
TPC-E-1185	Float Mandated by DOE Funding Profile Gap	13d	13-Oct-2016	31-Oct-2016	0d	$0.00
TPC-E-1200	Develop Test Plan	20d	01-Nov-2016	30-Nov-2016	0d	$18,502.80
TPC-E-1210	Distribute Test Plan and Boards to Coll	22d	01-Dec-2016	10-Jan-2017	0d	$2,120.00
TPC-E-1220	Test Boards by Collaborator ORNL / UT	26d	11-Jan-2017	16-Feb-2017	0d	$0.00
TPC-E-1230	Test Boards by Collaborator University of Houston	26d	11-Jan-2017	16-Feb-2017	0d	$3,837.60
TPC-E-1250	Test Boards by Collaborator - University of Bergen	26d	11-Jan-2017	16-Feb-2017	0d	$0.00
TPC-E-1260	Process University of Houston Subcontract Fee	1d	11-Jan-2017	11-Jan-2017	25d	$6,890.00
TPC-E-Mi17	Begin Testing by Collaborators	0d	11-Jan-2017		0d	$0.00
TPC-E-1270	Evaluate Collaboration Feedback	22d	17-Feb-2017	20-Mar-2017	0d	$20,561.60
TPC-E-Mi19	Complete Prototype Board - Rev. 0 (RR)	0d		20-Mar-2017	0d	$0.00



Discussion

- ALICE TPC, STAR iTPC, DREAM, VMM…
- We can borrow 512 channel proto-type board using DREAM. Some training and engineering
- I lost the T2K electronics discussion at some point. This electronics can be used for test purpose. Nikolai could report?
- We may want to decide based on timescale and costs (+ additional engineering effort to be needed)?

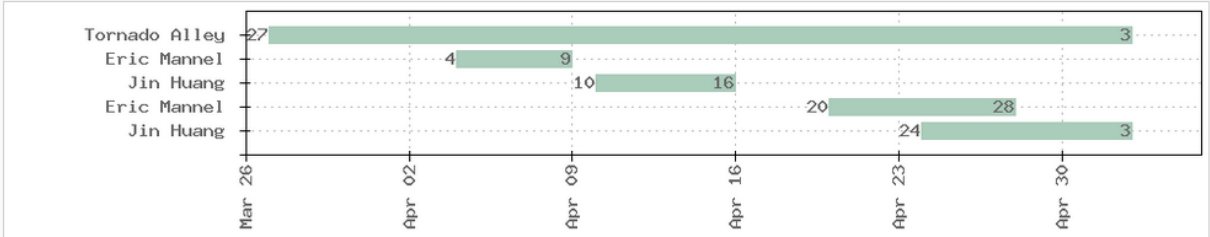
For beam test in April

- We have to collect people for supporting the proto-type TPC test
- Put your schedule
  - http://doodle.com/poll/xhs4daedwr822gdv

The current schedule for April T-1044 effort looks like this:

- March 28 to April 4: Receive the detector at FNAL, Set the detectors up outside the beam line enclosure and test electronics with the LED pulser system and cosmic rays.
- April 5-7: Move detectors into the beam line enclosure and obtain the ORC for operations
- April 8-11: Commission detectors in the beam, time in triggers, study the beam characteristics with the FTBF MPWC, Cerenkov detector and Pb-Glass detector.
- April 12-15: Study the EMCal performance with the detector located on the MT6.2-B motion table. Cosmic ray calibration of the HCal and parasitic studies of the HCal.
- April 16-18: Move EMCal out of beamline and study the HCal performance
- April 19-May 2: Place EMCal in front of HCal on support table.Study performance of the combined EMCal/HCal system.
- May 3: Rig the EMCal/HCal out of the MT6.2 area in perperation for modifications needed for the high rapidity tests to be carried out on November 2016.

For operations, a period coordinator with provide overall coordination of daily operations. During beam operations a minimum of 2 people are required to be at the facility. A present there are not specific shifts to sign up for. Daily shifts will be coordinated locally. The current calendar for people at FNAL is:



Temporary schedule of related people

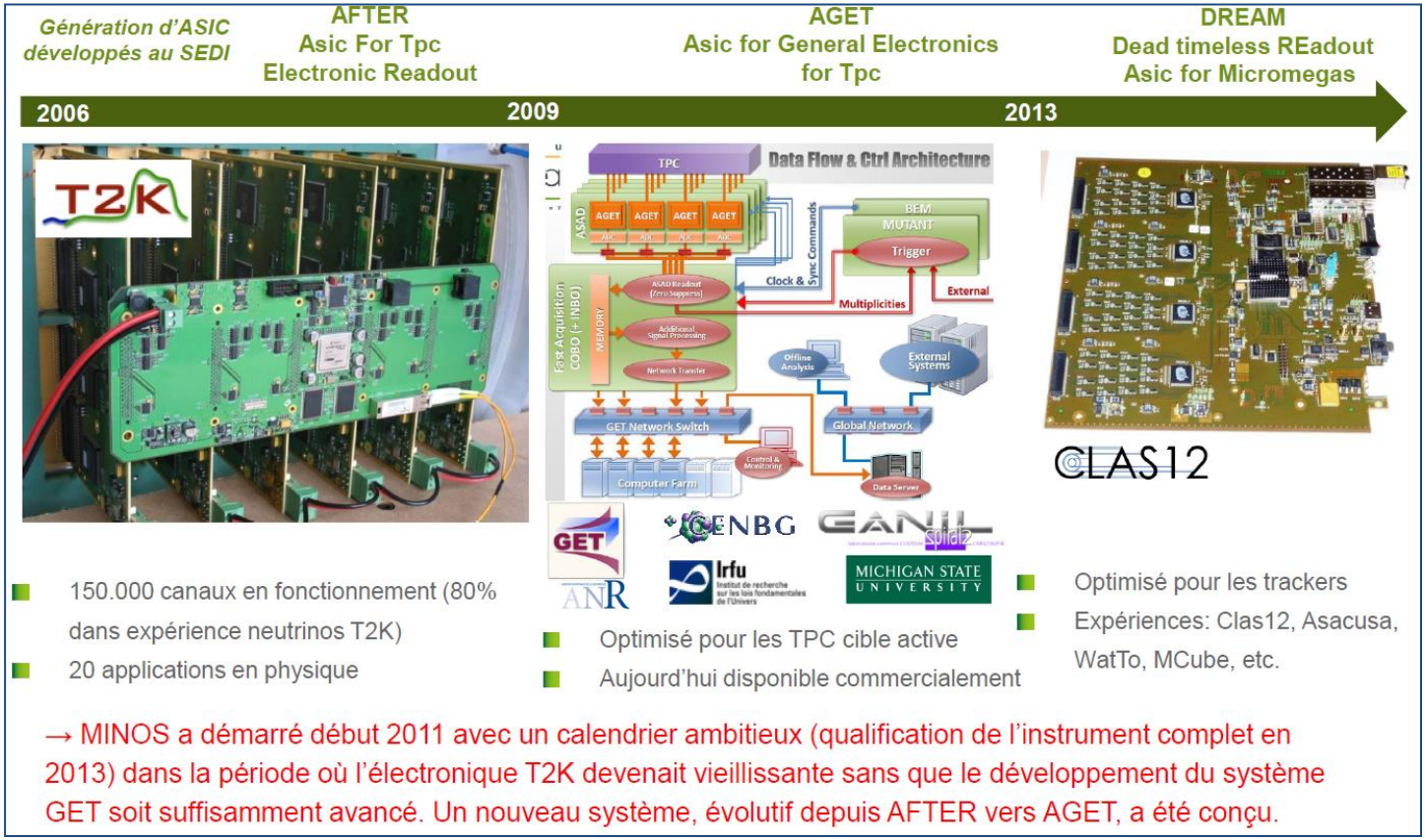
Craig Woody: 4/3-4/15, 4/24-5/2
Bob Azmoun: 4/3-4/15
Takao Sakaguchi: 4/17-4/24

backup

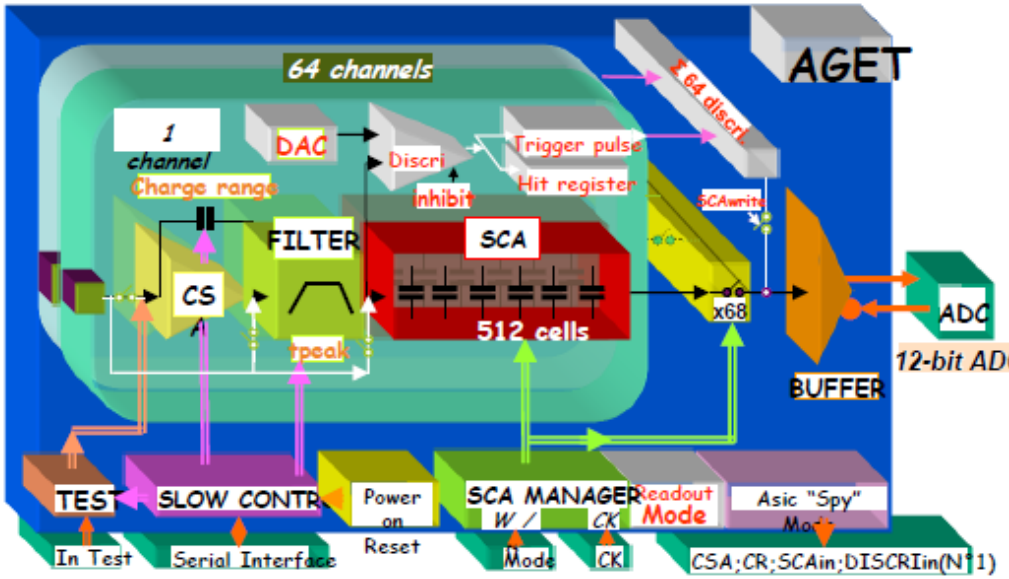
Let's DREAM? (but, for this R&D only?)

- Saclay Chips: AFTER → AGET → DREAM (Similar ingredient as SAMPA)

- With *AGET* chips, cost per channel is $40 (Craig's quote) → $8M for 200K channels -- three times more compared to ALICE TPC case ($2.5M)

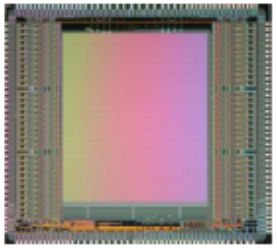


DREAM – successor of AGET



Caractéristiques

- Technologie: AMS CMOS 0,35 µm
- Surface: 8,5 x 7,6 mm^2
- 700,000 transistors
- Boîtier: LQFP 160 (28 x 28 x 1,4 mm)
- Production (jusqu'à 2014): 3200 chips



- **64 voies analogiques.** Pour chacune: *CSA, filtre, SCA (512 cells), Discriminateur*
- **Auto trigger :** discriminateur par canal + seuil commun grossier + seuil fin par canal
- **Signal de Multiplicité :** *somme analogique des discri. = nombre de canaux touchés*
- **Registre Hit Channel.** Accessible en lecture et écriture avant numérisation du SCA
- **Lecture du SCA:** *tout, canaux touchés, définis par l'utilisateur*
- **4 gammes de mesure:** *120 fC; 240 fC; 1 pC;10 pC (e.g. détecteurs Silicium)*
- **Polarité du signal d'entrée** *positive ou negative, définie par registre de configuration*
- **Bypass possible du CSA:** *permet d'utiliser un préampli/shaper externe*

Source: P. Baron